Charge pump with perfect current matching characteristics in phase-locked loops

Jae-Shin Lee, Min-Sun Keel, Shin-Il Lim and Suki Kim

Conventional CMOS charge pump circuits have some current mismatching characteristics. The current mismatch of the charge pump in the PLLs generates a phase offset, which increases spurs in the PLL output signals. In particular, it reduces the locking range in wide range PLLs with a dual loop scheme. A new charge pump circuit with perfect current matching characteristics is proposed. By using an error amplifier and reference current sources, one can achieve a charge pump with good current matching characteristics. It shows nearly perfect current matching characteristics over the whole VCO input range, and the amount of the reference spur is < –75dBc in the PLL output signal. The charge pump circuit is implemented in a 0.25μm CMOS process.

Introduction: A charge pump is widely used in modern phase-locked loops (PLL) for a low cost IC solution. Having a neutral state, an ideal charge pump combined with a phase/frequency detector (P/FD) provides an infinite DC gain with passive filters, which results in the unbounded pull-in range for second and higher order PLLs if not limited by the voltage controlled oscillator (VCO) input range [1]. As long as the P/FD and the charge pump are ideal, zero static phase error can be obtained. The charge pump, in general, shows nonideal characteristics when implemented in a circuit and its practical issues need to be considered in the design of the PLLs. One of the issues in the charge pump design is the current mismatch. In this Letter we consider the effects of the phase offset caused by the current mismatch and propose a new charge pump circuit with nearly perfect current matching characteristics.

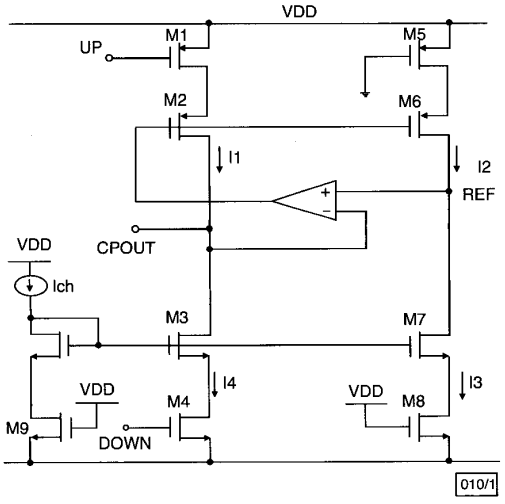

Fig. 1 *Proposed charge pump circuit*

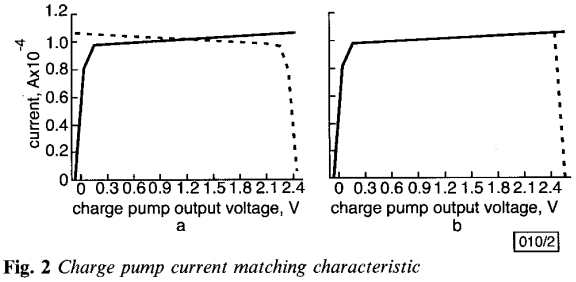

Fig. 2 *Charge pump current matching characteristic*

——— sinking
– – – sourcing
a Conventional charge pump
b Proposed charge pump

Charge pump design: CMOS charge pumps usually have UP and DOWN switches implemented with a PMOS FET and an NMOS FET, respectively. The conventional CMOS charge pump circuits have some current mismatching characteristics due to the difference between the drain-source voltage of the PMOS and NMOS FETs. The current mismatch of the charge pump in the PLLs generates a phase offset which increases spurs in the PLL output signals. Also, the phase offset reduces the locking range in the wide range PLL with the dual loop scheme frequency locking loop and phase locking loop, especially. When the current mismatch occurs in the charge pump, the amount of the phase offset is given by

$$\Phi_\varepsilon = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta_i}{I_{cp}} \quad \text{[rad]} \tag{1}$$

where Φ_ε, Δt_{on}, T_{ref}, I_{ep} and Δ_i are the phase offset, the turn-on time of the P/FD, the reference clock period, the charge pump current and the current mismatch of the charge pump, respectively. The amount of reference spur, P_r, in the third order PLL is given approximately by

$$P_r = 20\log\left[\frac{\sqrt{2}(I_{CP}R/2\pi)\Phi_\varepsilon K_{VCO}}{2f_{ref}}\right] - 20\log\frac{f_{ref}}{f_{pl}} \quad \text{[dBc]} \tag{2}$$

where R is the resistor value in the loop filter, K_{VCO} is the VCO gain, f_{ref} is the reference frequency for the P/FD and f_{pl} is the frequency of the pole in the loop filter [1]. As shown in eqn. 1, to minimise the phase offset, one should reduce the turn-on time of the P/FD and the current mismatch. The turn-on time of the P/FD, however, is needed a little to eliminate the dead-zone. So, we have to reduce the current mismatch as small as possible. In this Letter we propose a new charge pump circuit with nearly perfect current matching characteristics as shown in Fig. 1. For the conventional charge pumps, by enlarging the output impedance of the current source, the sourcing/sinking current matching is improved. This method, however, cannot produce perfect current matching characteristics because of the sizable output impedance of the practical devices used in the circuit. In the proposed charge pump, by using an error amplifier, the voltage V_{REF} at the node REF of the current mirror ($M5 \sim M8$) follows the voltage V_{CPOUT} at the node CPOUT of the charge pump ($M1 \sim M4$). As a result, the voltage V_{REF} is equal to the voltage V_{CPOUT} as long as the amplifier maintains a high enough gain. For $M5 = M1$, $M6 = M2$, $M7 = M3$ and $M8 = M4$, if the DOWN and the UP signal are high, then $I4 = I3 = I2$, and if the DOWN and the UP signal are low, then $I3 = I2 = I1$. So we can make the sinking current $I4$ equal the sourcing current $I1$. In this way, one can achieve nearly perfect source/sinking current matching characteristics regardless of the charge pump output voltages.

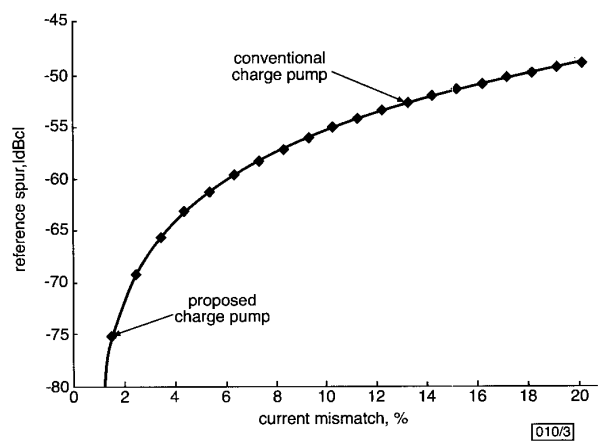

Fig. 3 *Reference spur against current mismatch*

Conditions: $I_{ep} = 100\mu A$, $f_{ref} = 5MHz$, $\Delta t_{on} = 50ns$, $K_{VCO} = 200MHz/V$, $f_{pl} = 16.5kHz$, $R = 7.5kW$

Fig. 2 shows the current variations against the output voltage variations of the charge pump circuit. For the conventional charge pump, perfect current matching occurs only when the output voltage of the charge pump, that is the input voltage of the VCO, is near the centre of the supply voltage. If the output voltage is near the supply voltage or the ground, the sourcing/sinking current difference is relatively large. For the proposed charge pump, the sourcing/sinking current matching is nearly perfect. For the same size of the transistors used in the circuit, the maximum difference

of the sourcing/sinking current in the conventional charge pump is > 13%, but the proposed charge pump has < 1% of that. Fig. 3 shows the amount of the reference spur against the variations of the current mismatch. While the conventional charge pump has a maximum reference spur of –52dBc, the proposed charge pump has a reference spur < –75dBc.

Conclusion: In this Letter we present a new charge pump with nearly perfect current matching characteristics in phase-locked loops. The current mismatch in the charge pump generates the phase offset which increases the spur in the PLL output signal and reduces the locking range in the wide range PLL. By using an error amplifier and a reference current source, we can achieve a charge pump which has nearly perfect current matching characteristics and the reference spur < –75dBc. It is implemented in a 0.25μm CMOS process and occupies an active area of 200 × 200μm.

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Discrete time small signal modelling of average current mode control

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A discrete time small signal modelling of an average current mode control is derived using the practical sampler model approach. By the practical sampler model approach, the small signal model structure can be simply defined. This model structure includes the two ideal samplers, which make it easy to obtain the discrete time model. To verify the usefulness of the proposed model, simulations and experiments are carried out.

Introduction: The average current mode control has been reported, and the superior characteristics over a peak current mode control such as good tracking performance of an average current, no slope compensation and noise immunity have been discussed [1]. In this control, the compensation network is presented in a current control loop to use the average current as a controlled quantity.

Although the design insights cannot be provided, the discrete time model is useful for understanding the behaviour of the power converter. Because of the presence of a compensation network, however, it is difficult to derive a discrete time small signal model of an average current mode using the conventional approach [2]. Thus, it is shown, in this Letter, that the derivation of a discrete time model of a current loop transfer function can be easily achieved using the practical sampler model approach.

Basic structure of proposed model: The circuit diagram of an average current mode controlled buck converter which is composed of a power stage, a compensation network and a modulator employing PWM is shown in Fig. 1. Because of the similarity of the modulator waveforms between peak and average current mode controls, the approach presented in [3] can be applied in discrete time small signal modelling of average current mode control. The effect of a compensation network, however, should be considered. Using the practical sampler model approach, the small signal model structure of an average current mode control can be drawn as in Fig. 2*a*. The different sampling instant of the two ideal sampler presented in this Figure can be unified with some manipulations including modification of compensation network. Fig. 2*b* shows the resultant small signal model structure.

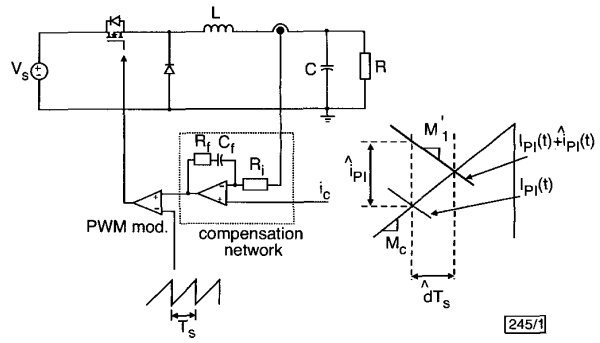

Fig. 1 *Circuit diagram of buck converter employing average current mode control*

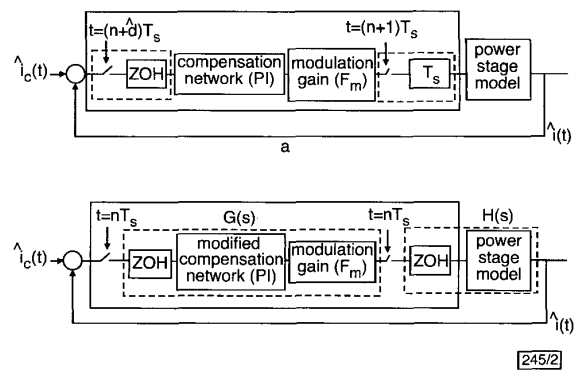

Fig. 2 *Model structure of average current mode control*

a Two samplers operate at different sampling instants
b Two samplers operate at same sampling instant

The sampling instant of an ideal sampler placed on a duty cycle generator is changed to that of the perturbed inductor current, and the modification of a compensator gain should be considered. For the model structure shown in Fig. 2*a*, the output value of a compensator is varied during the time interval of $t = (n + \hat{d})T_s$ and $t = (n + 1)T_s$. For a PI type compensation network, the variation can be expressed as

$$\Delta\hat{i}_{PI} = k_i(1 - \hat{d})T_s\hat{e} = k_iT_s\hat{e} - k_iT_s\hat{d}\hat{e} \qquad (1)$$

where $\hat{e}$ denotes the error signal between the perturbed reference and perturbed inductor currents. By assuming that the perturbed quantities are small, the second term on the right-hand side of eqn. 1 can be reduced to zero. To guarantee the equivalent condition of the perturbed inductor current at $t = (n + 1)T_s$ for the model structure shown in Fig. 2*b*, the compensation network should be modified from eqn. 1 as follows:

$$G'_{comp}(s) = k'_p + \frac{k_i}{s} \qquad (2)$$

where $k'_p = k_p + k_iT_s$. Note that, by the unification of two sampling instants of a practical sampler model, the modification of a compensation network should be carried out according to the equivalent condition of the perturbed inductor current at $t = (n + 1)T_s$ for the model structure shown in Fig. 2*b*.

Discrete time small signal model: From the small signal model structure shown in Fig. 2*b*, the discrete time model can be obtained. As an example, the buck converter is considered as a