Errata for the First Edition of *The Designer's Guide to Verilog-AMS*

Ken Kundert

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Contains a list of errors, corrections, and comments on the material presented in *The Designer's Guide to Verilog-AMS*.

Last updated on October 1, 2007. You can find the most recent version at www.designers-guide.org. Contact the author via e-mail at ken@designers-guide.com.

1 About the Errata

This paper contains a list of all the known errors in *The Designer's Guide to Verilog-AMS* [1]. It can be found on *The Designer's Guide* website [2]. In addition, this website also contains the most recent versions of all of the examples from the book.

Please report any errors you find in this book to *dg-ams@designers-guide.org* for inclusion in this errata.

2 Errata for Front Matter

None.

3 Errata for Chapter 1: Introduction

None.

4 Errata for Chapter 2: Top-Down Design

None.

5 Errata for Chapter 3: Analog Modeling

In this chapter, all references to *discipline.vams* should be changed to *disciplines.vams.* They include:

1. Twice on page 41 in the first paragraph or Section 2.
2. On page 92 in Listing 28.
3. On page 93 in Listing 29.
4. On page 97 in Listing 30.

5.1 Section 2: A Simple Circuit

5.1.1 Listing 7 and 8, pg. 43 and 48

When declaring the ground, the node that is to act as ground must already be declared. Thus, it is necessary to specify the discipline of ground before declaring it to be ground. In both of these listings, the ground statement should be replaced by the following:

```
electrical gnd;
ground gnd;
```

5.2 Section 3: Motor

5.2.1 Listing 9, pg. 51

Issue. In the module *test*, the line that instantiates the motor model is incorrect.

```
motor M1 (drive, gnd, shaft);
```

The order of the nodes does not match the order of the corresponding ports in the module *motor*.

Submitted independently by Gregg Kodra and Henry Chang on 29 August 2005.

Correction. This line should be changed to:

```
motor M1 (shaft, drive, gnd);
```

5.3 Section 6.1: Non-Ideal Relay

5.3.1 Listing 18, pg. 70

Issue. In the module *relay*, the line that defines the *goff* parameter is incorrect.

```
parameter real goff=0 from [0:/1ron);     // off conductance (Siemens)
```

The upper range limit is garbled.

Submitted by Geoffrey Coram on 1 October 2007.

Correction. This line should be changed to:

```
parameter real goff=0 from [0:1/(1+ron));     // off conductance (Siemens)
```

5.3.2 Listing 19, pg. 71

Issue. In the module *relay*, the line that defines the *goff* parameter is incorrect.

```
parameter real goff=0 from [0:/1ron);     // off conductance (Siemens)
```

The upper range limit is garbled.

Submitted by Geoffrey Coram on 1 October 2007.

Correction. This line should be changed to:

```
parameter real goff=0 from [0:1/ron);          // off conductance (Siemens)
```

5.4 Section 10: Analog to Digital Converter

5.4.1 Listing 26, pg. 85

Issue. In the module *adc*, the declaration for the array *result* is incorrect.

```
integer result[0:bits–1];
```

It should be a real array rather than an integer array.

Submitted by Jaime E. Kardontchik on 19 November 2005.

Correction. This line should be changed to:

```
real result[0:bits–1];
```

6 Errata for Chapter 4: Mixed-Signal Modeling

6.1 Section 4.2.1: Basic Mixed-Signal Discipline Resolution

6.1.1 Figure 5, pg. 127

Issue. In the blocks *d4* and *d6* the discipline of the pins is given as *logic_a*. These do not match the description given in the text..

Correction. This discipline of the pin on *d4* should be changed to *logic_b* and the discipline of the pin on *d6* should be changed to *logic*.

6.2 Section 4.2.2: Detailed Mixed-Signal Discipline Resolution

6.2.1 Figure 6, pg. 128

Issue. In the blocks *d4* and *d6* the discipline of the pins is given as *logic_a*. These do not match the description given in the text..

Correction. The discipline of the pin on *d4* should be changed to *logic_b* and the discipline of the pin on *d6* should be changed to *logic*.

6.3 Section 4.2.3: Automatic Connect Module Insertion

6.3.1 Figure 7, pg. 129

Issue. In the blocks *d4* and *d6* the discipline of the pins is given as *logic_a*. These do not match the description given in the text..

Correction. The discipline of the pin on *d4* should be changed to *logic_b* and the discipline of the pin on *d6* should be changed to *logic*.

7 Errata for Chapter 5: Language Reference

7.1 Section 2.5: Ports, Nets, and Nodes

7.1.1 Page 166

When declaring the ground, the node that is to act as ground must already be declared. Thus, it is necessary to specify the discipline of ground before declaring it to be ground. In the example in the middle of this page, the ground statement should be replaced by the following:

```
electrical gnd;
ground gnd;
```

7.2 Section 7.6.8: Z Transform Filters

7.2.1 Paragraph 2, pg. 184

Issue. The text "The first is the input signal, $y(t)$." is incorrect in that $y(t)$ is not the input signal.

Correction. The text should read "The first is the input signal, $x(t)$."

7.3 Section 6.8.3: Threshold Crossings

7.3.1 Listing 4: Warn on Breakdown, pg 208

Issue. Example is not compliant with Verilog-AMS LRM 2.1 in two respects:

1. It uses the @above event, which is not described in the LRM and only available in Cadence simulators.
2. It uses a string parameter, which is not allowed in version 2.1 of Verilog-AMS.

Also, the version of this example given on the website (*ch5/listing05.tar.gz*) contains a file *breakdown2.vams* that is not used in the example.

Submitted by Geoffrey Coram on 3 June 2004.

Correction. The @above event is not contained in version 2.1 of the Verilog-AMS LRM (language reference manual). However, it has been submitted to the committee and is expected to be in version 2.2.

String parameters are not explicitly described in the LRM, however there is ambiguity in the definition of the language that allows many simulators to support them. Recall that in Verilog-HDL the parameter types are not explicitly declared, but rather take their type from the value they are set to. Verilog-A added the concept of explicitly declared parameter types, but only allowed explicitly declaring reals and integers. This is being corrected in verilog 2.2 of the LRM with the addition of *string* parameter types. Until then, many implementations allow strings to be passed if the type of the parameter is not explicitly declared.

The file *breakdown2.vams* is an alternative to *breakdown.vams* that is provided because *breakdown.vams* does not work properly on all implementations.

8 Errata for Appendix A: Compatibility

None.

9 Errata for Back Matter

None.

10 If You Have Questions

If you have questions about what you have read in the book, feel free to post them on the *Forum* section of *The Designer's Guide Community* website. Do so by going to *www.designers-guide.org/Forum*.

References

[1] Kenneth S. Kundert and Olaf Zinke. *The Designer's Guide to Verilog-AMS (first edition)*. Kluwer Academic Publishers, 2004.

[2] *The Designer's Guide*. *www.designers-guide.org*.