Simulating the Phase Noise Contribution of the Divider in a Phase Lock Loop

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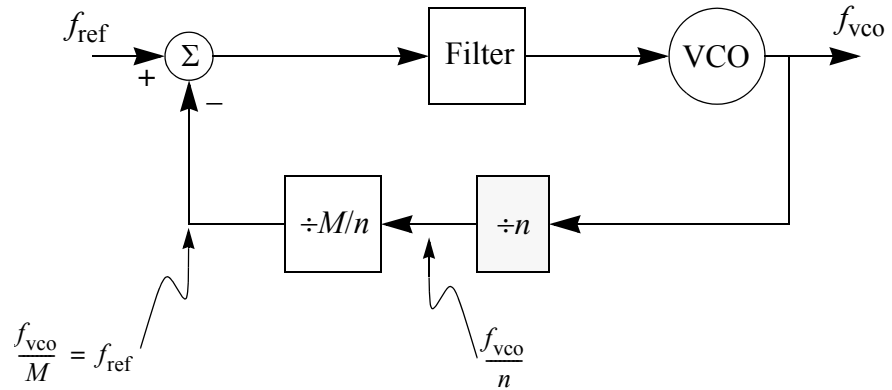
Version 1, 23 May 2003   Describes a process for determining the amount of phase noise contributed to the output of a PLL-based frequency synthesizer by the frequency divider.
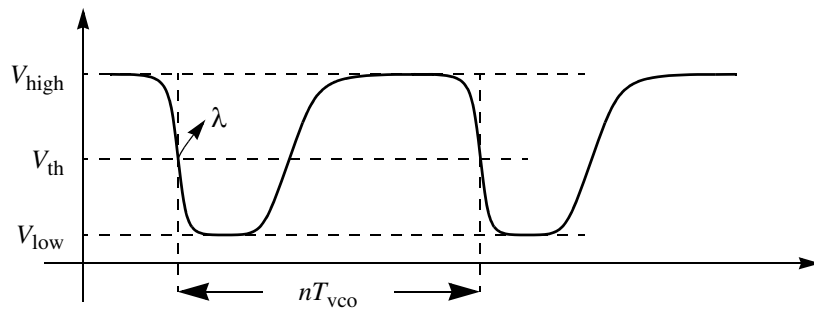
Consider the PLL shown in Figure 1 that multiplies the reference frequency by M. We want to simulate the contribution of part of the divider, for example the first divide-by-n, to the output phase noise.

FIGURE 1   *A PLL with divide ratio of M.*

The VCO oscillates at frequency f_{vco} and the divider output is a periodic waveform of frequency f_{vco}/n, as shown in Figure 2. The next stage is usually triggered by one of the two edges of this waveform, either the rising or the falling, and for this reason only this edge deserves further attention. More specifically we consider that the next stage is triggered when the divider output crosses some threshold voltage V_{th}, which for CMOS gates is usually close to half of the supply voltage. Because of device noise and possibly from interference from other on chip signals the edge of interest is noisy, that is it triggers the next stage at some time instant different than the ideal. This time error is a discrete time random process, and we will denote its power spectral density (PSD) with $S_{t,f_{vco}/n}(f)$.

FIGURE 2   *The waveform at the divide-by-n output.*

The divide-by-n is a periodically-time-varying circuit and can be simulated with SpectreRF. PSS analysis with fundamental frequency f_{vco}/n can be used to find the steady state waveforms, and the new strobed PNoise analysis can be used to find the noise in terms of voltage at the time instant that the edge of interest of the output waveform crosses the threshold voltage V_{th}. SpectreRF provides the PSD of this discrete time random process with voltage units, which will be denoted here with $S_{V,f_{vco}/n}(f)$. The PSD of the time error is related to the voltage error PSD as follows

$$S_{t,f_{\mathrm{vco}}/n}(f) = \frac{1}{\lambda^2} S_{V,f_{\mathrm{vco}}/n}(f) \tag{1}$$

where λ is the slope of the divide-by-n output at the instant that it crosses V_{th}, and it can be measured from the divider output waveform
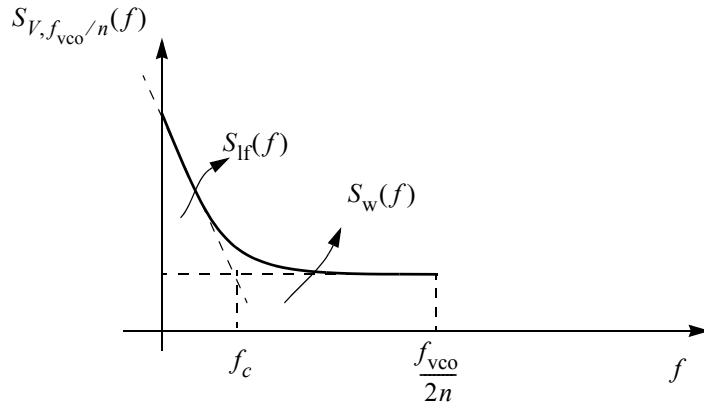
$$\lambda = \frac{dV_{\mathrm{out}}}{dt}\bigg|_{V_{\mathrm{out}} = V_{\mathrm{th}}} \tag{2}$$

Typically $S_{t,f_{\mathrm{vco}}/n}(f)$ and $S_{V,f_{\mathrm{vco}}/n}(f)$ have a white noise part and a low frequency noise part above the white noise that is caused by device flicker noise, as shown in Figure 3

$$S_{V,f_{\mathrm{vco}}/n}(f) = S_{\mathrm{lf}}(f) + S_{\mathrm{w}}(f) \tag{3}$$

These PSDs are periodic in frequency with period f_{vco}/n. Because they are also even functions of frequency, only the part up to $f_{\mathrm{vco}}/(2n)$ for positive frequencies is shown in Figure 3.

FIGURE 3   *A noise spectrum that contains both white noise (S_{w}) and low frequency flicker noise (S_{lf}).*

The signal at the output of the divide-by-n is further divided by M/n to form the feedback signal at the input of the loop.

In general, division by K in the time domain means that one of every K edges is being transferred to the output and $K - 1$ are being swallowed. This undersampling in the time domain is folding in the frequency domain. In the general case

$$S_{\mathrm{out}}(f) = \sum_{i=0}^{K-1} S_{\mathrm{in}}\left(f - \frac{i}{KT_{\mathrm{in}}}\right) \tag{4}$$

where $S_{\mathrm{in}}(f)$ and $S_{\mathrm{out}}(f)$ represent the PSD of the timing error at the input and the output of the divider and T_{in} is the period of the input signal.

Applying (4), the PSD of the noise signal $S_{t,f_{\mathrm{vco}}/M}(f)$ at the input of the loop at frequency f_{vco}/M can be calculated. The phase noise at the input signal is:

$$S_{\phi, f_{\text{vco}}/M}(f) = \left(\frac{2\pi}{MT_{\text{vco}}}\right)^2 S_{t, f_{\text{vco}}/M}(f) \tag{5}$$

The corresponding in band phase noise at the PLL output is

$$S_{\phi, f_{\text{vco}}}(f) = M^2 S_{\phi, f_{\text{vco}}/M}(f) = \left(\frac{2\pi}{T_{\text{vco}}}\right)^2 S_{t, f_{\text{vco}}/M}(f) \tag{6}$$

Depending on the relation between the corner frequency f_{c} at which $S_{\text{lf}}(f)$ and $S_{\text{w}}(f)$ intersect and the reference frequency of the PLL, the low frequency part is usually not subject to aliasing from the folding described by (4). Therefore, denoting the PSDs of the low frequency noise with "lf"

$$S_{t, f_{\text{vco}}/M}^{\text{lf}}(f) = S_{t, f_{\text{vco}}/n}^{\text{lf}}(f) \tag{7}$$

and

$$S_{\phi, f_{\text{vco}}}^{\text{lf}}(f) = \left(\frac{2\pi f_{\text{vco}}}{\lambda}\right)^2 S_{\text{lf}}(f) \tag{8}$$

The white noise part however is being aliased and as a result the magnitude of the PSD of the divided signal is being increased by the divide ratio M/n, or

$$S_{t, f_{\text{vco}}/M}^{\text{w}}(f) = (M/n) S_{t, f_{\text{vco}}/n}^{\text{w}}(f) \tag{9}$$

where the superscript "w" denotes the white noise part. The corresponding output phase noise is

$$S_{\phi, f_{\text{vco}}}^{\text{w}}(f) = \frac{M}{n}\left(\frac{2\pi f_{\text{vco}}}{\lambda}\right)^2 S_{\text{w}}(f) \tag{10}$$

Finally, the total output phase noise is

$$S_{\phi, f_{\text{vco}}}(f) = \left(\frac{2\pi f_{\text{vco}}}{\lambda}\right)^2 \left(\frac{M}{n} S_{\text{w}}(f) + S_{\text{lf}}(f)\right) \tag{11}$$

The same approach can be applied to find the phase noise contribution of other circuits in the feedback path and the input of the loop, such as clock buffers and the phase frequency detector.

If you have questions about what you have just read, feel free to post them on the *Forum* section of *The Designer's Guide* website. Do so by going to *www.designers-guide.org/ Forum*.